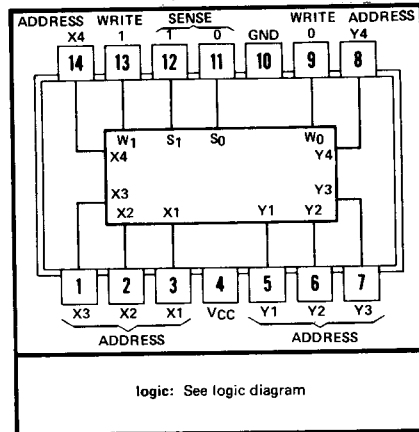## description

Each of these 16-bit active-element memories is a high-speed, monolithic, transistor-transistor-logic (TTL) array of 16 flip-flops and two write amplifiers interconnected to form a scratch-pad memory with direct-address and nondestructive read-out. These devices are interchangeable with and replace SN5481, SN7481, SN5484, and SN7484, but feature diode-clamped inputs, improved switching speeds, and lower supply current requirements.

The flip-flops are arranged in a four-by-four matrix with each flip-flop representing one bit of 16 words. Four X-address lines and four Y-address lines permit the address of one bit at a time. Each flip-flop, composed of two cross-coupled three-emitter transistors, is used to store one bit. To determine if a logic 1 or logic 0 has been stored, it is necessary to know which one of the two flip-flop transistors is conducting. One emitter of each of these transistors serves as the sensing output. All 16 of the logic 1 sensing outputs are connected to the sense 1 (S_1) amplifier input and all 16 of the logic 0 sensing outputs are connected to the sense 0 (S_0) amplifier input. The two remaining emitters of each transistor are used to complete the matrix connections necessary for the X- and Y-address lines. Address line inputs are normally held low and currents from all conducting flip-flop transistors flow out of these address lines.
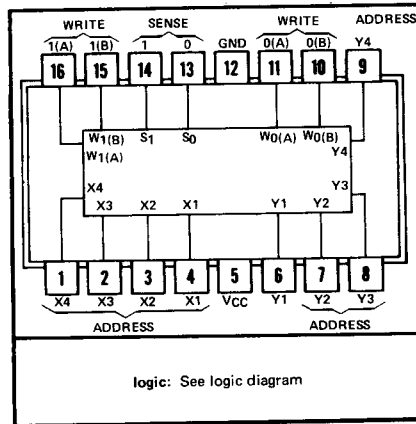
To address a flip-flop both the X- and Y-address lines associated with that flip-flop are taken to a high level. Due to the matrix nature of the circuit, at least one address line of all flip-flops except the one being addressed will continue to remain at a low level and no change will occur in those flip-flops. But, in the addressed flip-flop, the current in the conducting transistor diverts from the address lines to the appropriate sense line and then to one of the sense amplifiers. Thus, either the sense 1 amplifier or the sense 0 amplifier is activated. When this occurs, the output of the activated sense amplifier drops from a high logic level to a low logic level. The memory is nondestructive as the states of the flip-flops are not disturbed during sensing. The memory is volatile and information will be lost if the supply voltage is removed.

SN5481A ... J OR W PACKAGE
SN7481A ... J OR N PACKAGE
(TOP VIEW)

logic: See logic diagram

SN5484A ... J OR W PACKAGE
SN7484A ... J OR N PACKAGE
(TOP VIEW)

logic: See logic diagram

To store new information in a flip-flop, it is necessary to address it and apply a high-level voltage to the appropriate write amplifier. (The SN5484A and SN7484A have gated write-amplifier inputs). The output of the write amplifier responds by dropping to a low logic level. Since all Sense 0 lines are connected to the output of the write 0 amplifier and all sense 1 lines are connected to the output of the write 1 amplifier, a low level at the output of a write amplifier

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description (continued)

will cause the emitters of all flip-flop transistors connected to that amplifier to go low. In all the flip-flops except the one being addressed, this low voltage has no effect since at least one other emitter on each of the flip-flop transistors is held low by the address lines. Two possibilities exist with the flip-flop that is addressed. The flip-flop may already be in the desired state, in which case no change occurs. If the flip-flop must be changed from one state to the other, the low voltage applied to the emitter of the transistor which is not conducting turns that transistor on causing the other transistor to turn off.

Since the connection between the output of the write amplifier and the sense line is common to the input of the sense amplifier, the memory cannot be used to provide information on the state of a bit while the write amplifiers are activated.

A number of active-element memories may be paralleled to form the desired matrix size (number of words) and to form the desired word length (number of bits). All inputs and outputs are compatible with most DTL and TTL circuits. Average power dissipation is typically 225 milliwatts, and the open-collector outputs may be wire-AND connected to similar outputs. Internal circuitry of the write and sense amplifiers are operated within their linear range to improve speed. Sensing propagation delay times are typically 12 nanoseconds when operated at full fan-out and 30 picofarads of circuit capacitance. The SN5481A and SN5484A circuits are designed for operation over the full military temperature range of $-55°C$ to $125°C$; the SN7481A circuits are designed for operation from $0°C$ to $70°C$.

logic diagram

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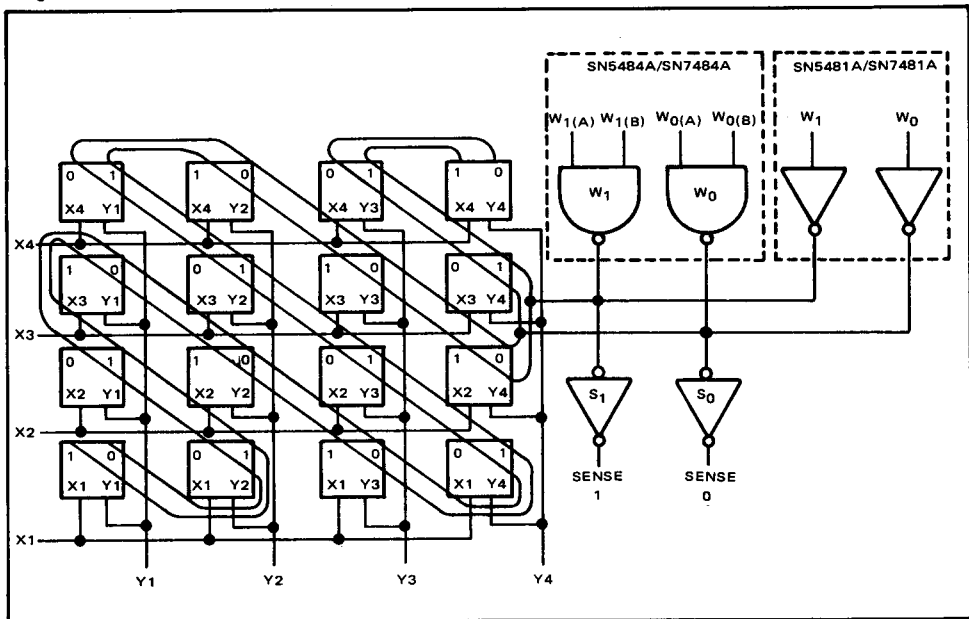
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 2)	5.5 V
High-level output voltage	5.5 V
Operating free-air temperature range: SN5481A, SN5484A Circuits	-55°C to 125°C
SN7481A, SN7484A Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to any X input in conjunction with any Y input.

recommended operating conditions

	SN5481A, SN5484A			SN7481A, SN7484A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			20			40	mA
Width of write pulse, $t_{w(write)}$ (see Figure 1)	20			20			ns
Address input setup time, t_{su} (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN5481A, SN5484A			SN7481A, SN7484A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level voltage at any input		2			2			V
V_{IL}	Low-level voltage to prevent writing at address inputs				0.8			0.8	V
	to prevent sensing				1			1	
V_{IL}	Low-level voltage at write inputs				0.8			1	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = -12 mA			-1.5			-1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{OH} = 5.5 V			250			250	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = MAX			0.4			0.4	V
I_I	Input current at maximum input voltage Write	V_{CC} = MAX,V_I = 5.5 V			1			1	mA
	Address				3			3	
I_{IH}	High-level input current Write	V_{CC} = MAX,V_I = 2.4 V			40			40	μA
	Address	V_{CC} = MAX,V_I = 4.5 V			400			400	
I_{IL}	Low-level input current Write	V_{CC} MAX, V_I = 0.4 V			-1.6			-1.6	mA
	Address				-11			-11	
I_{CC}	Supply current	V_{CC} = MAX,All inputs at 0 V			70			65	mA
		V_{CC} = 5 V, All inputs at 0 V	45	60		45	60		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

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switching characteristics, V_{CC} = 5 V, I_{OL} = MAX[†], T_A = 25°C, see figure 1

| PARAMETER[§]	LOCATION ADDRESSED	TEST CONDITIONS	SN5481A, SN5484A			SN7481A, SN7484A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{SR}	X1 – Y1	C_L = 30 pF		13			13		ns
		C_L = 200 pF		18	30		18	30	
t_{PHL}	X1 – Y1	C_L = 30 pF		11	19		12	20	ns
		C_L = 200 pF		17	26		18	27	
t_{PLH}		C_L = 30 pF		13	20		12	19	
		C_L = 200 pF		27	40		18	27	
t_{PHL}	X1 thru X4 and Y1	C_L = 30 pF		10	18		11	19	ns
		C_L = 200 pF		16	25		17	26	
t_{PLH}		C_L = 30 pF		13	20		13	20	
		C_L = 200 pF		27	40		19	28	

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

[§]t_{SR} ≡ Sense recovery time after writing

t_{PHL} ≡ Propagation delay time, high-to-low-level output

t_{PLH} ≡ Propagation delay time, low-to-high-level output

schematic
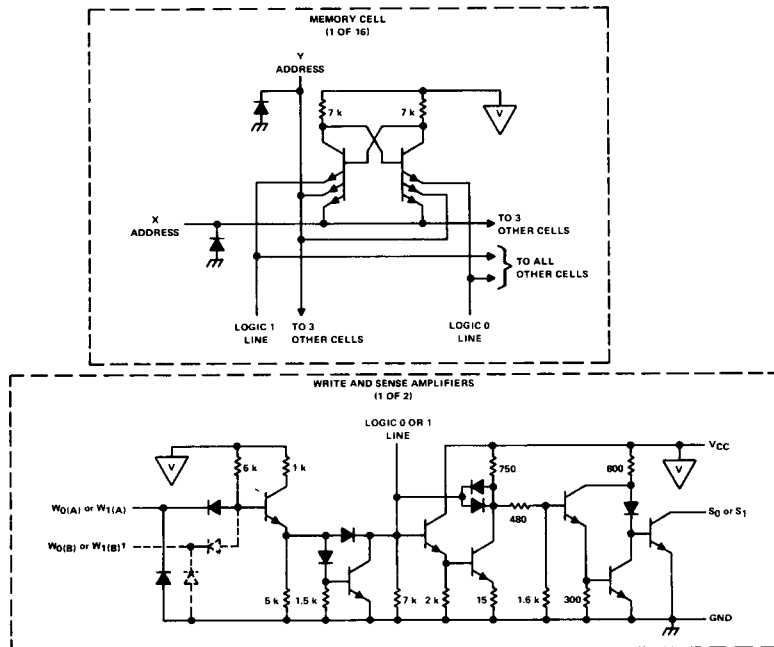
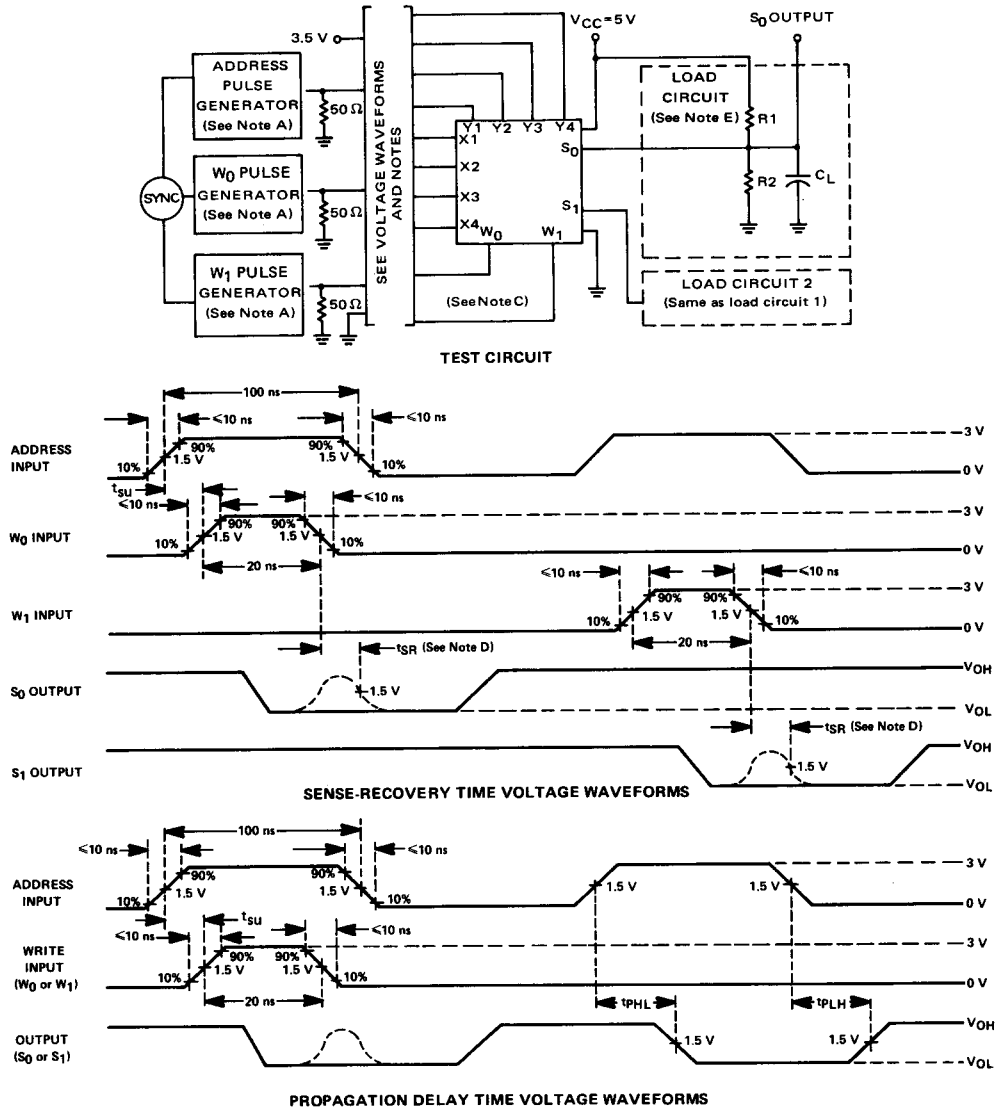[†]$W_{0(B)}$ and $W_{1(B)}$ inputs (indicated with dashed lines) are applicable for the SN5484A, SN7484A only.

▽ . . . V_{CC} bus

Resistor values shown are nominal and in ohms.

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PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT

SENSE-RECOVERY TIME VOLTAGE WAVEFORMS

PROPAGATION DELAY TIME VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: for the address pulse generator, PRR = 2 MHz; for the W_0 and W_1 pulse generators, PRR = 1 MHz.
   B. C_L includes probe and jig capacitance.
   C. For the SN5484A and SN7484A, unused W_0 and W_1 inputs are at 3.5 V.
   D. $t_{SR} \equiv$ sense-recovery time
   E. For the SN5481A and SN5484A: R1 = 240 Ω and R2 = 560 Ω. For the SN7481A and SN7484A: R1 = 120 Ω and R2 = 330 Ω.

FIGURE 1–SWITCHING CHARACTERISTICS